## REMARKS

The foregoing amendments to Claim 23 are necessary to conform the claim with the disclosure. Claim 23 is exemplified by the embodiment of Fig. 24. Referring to that figure, the claimed first bit line pair is exemplified by lines BL[n], /BL[n], the claimed second bit line pair is exemplified by lines LBL[n], /LBL[n], and the claimed first and second MOSFETs are exemplified by transistors M206a and M207a. As is apparent, each MOSFET has a source-drain path coupled to one line from each bit line pair. The present amendments correct an inconsistency between the previous language of Claim 23 and the disclosed arrangement of the MOSFETs.

The present amendments do not change the scope of Claim 23 as exemplified by the disclosure, and accordingly should not require additional search or examination. Moreover, Claim 23 remains patentable for the same reasons as set forth in the Examiner's Statement of Reasons for Allowance, properly interpreted in light of the disclosure. The amendments could not have been presented earlier, because the inconsistency with the disclosure was inadvertent and was not recognized prior to allowance of the application.

Accordingly, entry of this Amendment is believed to be appropriate, and is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16

and 1.17 that may be required by this paper and to credit any overpayment to that Account.

Respectfully submitted,

MWS:sjk

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April 11, 2005

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## **CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mall in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

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